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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,800	03/30/2004	Shoichiro Matsumoto	YKI-0148	7558

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EXAMINER	
MA, CALVIN	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,800	MATSUMOTO, SHOICHIRO	
	Examiner	Art Unit	
	Calvin Ma	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :03/30/2004, 06/16/2004, 05/01/2006, 05/11/2006.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim1, 4 of U.S. App. No. 10/872347. Although the conflicting claims are not identical, they are not patentably distinct from each other for the reasons below.

Claims 1 and 4 of the application 10/872347	Claim 1 of the application 10/813800
(Claims 1) A display device for presenting display using a current video signal, comprising: a voltage-current conversion circuit for converting a voltage video signal into a current video signal; and a current driving pixel circuit for receiving the current video signal output from said voltage-current conversion circuit to present display, wherein said voltage-current conversion circuit includes an output transistor for receiving the voltage video signal at a gate, and supplying corresponding drain current, and a compensation circuit for compensating for variation in threshold voltage of said output transistor.	A display device performing display including an emissive element in each of pixels arranged in a matrix, comprising : a voltage-to-current conversion circuit for converting an externally supplied voltage video signal indicating a display luminance for each pixel into a current video signal;
(Claims 4) wherein said compensation circuit includes a storage capacitor for receiving at one end and holding a data voltage supplied to the gate of said output transistor, a first control signal line connected to the other end of said storage capacitor, and receiving a predetermined voltage or a pulsed signal,	a data line connected to the voltage-to-current conversion circuit for sequentially receiving therefrom the current video signal for pixels along a vertical direction; and a pixel circuit connected to the data line, in which a voltage in accordance with the current video signal supplied in the data line is retained in an auxiliary capacitor, and a current corresponding to the voltage retained in the auxiliary capacitor is made to flow in a drive element, so as to cause light emission in a corresponding emissive element.

Note the comparison above, claim 1 of the instant application is not patentably distinct from claims 1 and 4 of the U.S. App. No. 10/872347. For example, claim 1 of the application is broader than claim 1 and 4 of the U.S. App. No. 10/872347 by deleting the limitation "compensating for variation". Thus, it would be obvious to one of ordinary skill in the art at the time the invention was made to have removed the limitation "compensating for variation" in claims 1 and 4 of the U.S. App. No. 10/872347 where the functionality is not needed.

Claims 2-10 are rejected to as being dependent upon a rejected base claim 1.

4. Claims 1-10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1,7 of U.S. App. No. 10/8331803. Although the conflicting claims are not identical, they are not patentably distinct from each other for the reasons below.

Claims 1, 7 of the application 10/8331803	Claim 1 of the application 10/813800
(Claims 1) A display device having an emissive element in each of pixels arranged in a matrix form and in which a display is achieved, the display device comprising a data line to which a data current is supplied from the video data processor circuit;	A display device performing display including an emissive element in each of pixels arranged in a matrix, comprising:
a video data processor circuit for receiving both a voltage signal and a current video signal for a pixel, storing a voltage when a current corresponding to the current video signal is supplied, and outputting a data current corresponding to the stored voltage; and a pixel circuit connected to the data line for storing a voltage corresponding to a data current flowing on the data line and for driving a driver element based on the stored voltage to allow the emissive element to emit light.	a pixel circuit connected to the data line, in which a voltage in accordance with the current video signal supplied in the data line is retained in an auxiliary capacitor, and a current corresponding to the voltage retained in the auxiliary capacitor is made to flow in a drive element, so as to cause light emission in a corresponding emissive element.
(Claims 7) A display device according to claim 1, further comprising: a current-to-voltage converter circuit for outputting, based on a data current output from the video data processor circuit, a voltage signal for corresponding data line, wherein the current-to-voltage converter circuit supplies the voltage signal for data line and the data current to the data line.	a voltage-to-current conversion circuit for converting an externally supplied voltage video signal indicating a display luminance for each pixel into a current video signal; a data line connected to the voltage-to-current conversion circuit for sequentially receiving therefrom the current video signal for pixels along a vertical direction;

Note the comparison above, claim 1 of the instant application is not patentably distinct from claims 1 and 7 of the U.S. App. No. 10/8331803. For example, claim 1 of the application is broader than claim 1 and 7 of the U.S. App. No. 10/8331803by deleting the limitation "stored voltage". Thus, it would be obvious to one of ordinary skill in the art at the time the invention was made to have removed the limitation "stored voltage" in claims 1 and 7 of the U.S. App. No. 10/8331803 where the functionality is not needed.

Claims 2-10 are rejected to as being dependent upon a rejected base claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3-6, rejected under 35 U.S.C. 102(e) as being anticipated by Kimura (US Patent 7,138,967).

Consider claim 1, Kimura discloses a display device for performing display including an emissive element in each of pixels arranged in a matrix (see Fig. 1, 3, 14), comprising:

a voltage-to-current conversion circuit (101) for converting an externally supplied voltage video signal indicating a display luminance for each pixel into a current video signal (see Fig. 3A, 4, where the switching element 101 as the "voltage-to-current conversion circuit" by inputting the voltage based video signal and output current to the driving element Col.9, Line 37-40, Col.17, Line 57-67);

a data line(see Fig 5, W) connected to the voltage-to-current conversion circuit(101) for sequentially receiving therefrom the current video signal for pixels along a vertical direction(the data line W is indirectly connected to the switching element 101 to receive the signal sequentially); and

a pixel circuit (302) connected to the data line, in which a voltage in accordance with the current video signal supplied in the data line is retained in an auxiliary capacitor (303), and a current corresponding to the voltage retained in the auxiliary capacitor (303) is made to flow in a drive element(302), so as to cause light emission in a corresponding emissive element(106) (Col.21, Line10-21).

Consider claim 3, Kimura teaches a device as defined in claim 1, wherein the voltage-to-current conversion circuit (101) comprises:

an output transistor (301) which receives the voltage video signal at its control terminal and outputs to the data line a current in accordance with the voltage video signal (Col.21, Line10-21).

Consider claim 4, Kimura teaches a device as defined in claim 3, wherein the voltage-to-current conversion circuit (101) further comprises:

a capacitor (303) for retaining the voltage video signal supplied to the control terminal of the output transistor (Col.21, Lines 7-14).

Consider claim 5, Kimura teaches a device as defined in claim 3, wherein

the drive element (302) and the output transistor(301) of the voltage-to-current conversion circuit (101) are of opposite conduction types (Col.21, Lines 15-21).

Consider claim 6 Kimura teaches a device as defined in claim 1, wherein the voltage-to-current conversion circuit comprises:

a capacitor(303) for retaining a voltage in accordance with the voltage video signal; and

an output transistor(301) for outputting a current in accordance with the voltage retained in the capacitor (Col.21, Lines 7-14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7-10 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 7,138,967 to Kimura in view of Chen. (U.S.P.G. Pub. 2003/0184510)

Consider claim 7, Kimura teaches the display element in claim 6, Kimura does not teach first and second capacitors each for retaining a voltage in accordance with the voltage video signal; first and second output transistors for outputting a current in accordance with the voltage retained in the first and second capacitors, each of the first and second output transistors receives at its control terminal a charge voltage of the corresponding one of first or second capacitors; has one controlled terminal connected to a power source; and one other controlled terminal connected to the data line; while the signal is supplied if the input switching circuit to the first capacitor, the output switching circuit to the second capacitor, the output switching circuit supplies the current from the first output transistor to the data line; wherein the

first and second output transistors are connected to the power source via separate lines. Chen (Fig. 7-8) teaches first (6031) and second capacitors (602) each for retaining a voltage in accordance with the voltage video signal; first and second output transistors for outputting a current in accordance with the voltage retained in the first and second capacitors [0039] (the two switching transistor each having a capacitor for storage); has one controlled terminal connected to a power source(VCOM); and one other controlled terminal (BS) connected to the data line (see Fig 6); while the signal is supplied if the input switching circuit to the first capacitor (6031), the output switching circuit to the second capacitor (602), the output switching circuit supplies the current from the first output transistor(701) to the data line; wherein the first and second output transistors(702) are connected to the power source via separate lines.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the double capacitor and double transistor structure of Chen with the pixel driving circuit of Kimura since it allows "effective blanking function to promote OLED performance" (Chen [0039]).

Allowable Subject Matter

9. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

It is found that the prior art U.S.P.G. Pub. 2004/0017162 also teaches the double capacitor, double transistor and would also be able to combine with Kimura under 103. Also the application was found to be very similar to U.S.P.G. Pub. 2004/0207617 by the applicant but not to the degree of a non-obvious double patenting.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is (571)270-1713. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C. Ma
February 16, 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER